COMMUNICATION DEVICE FOR TRANSMITTING MESSAGE SIGNALS

The invention relates to a communication device according to the preamble of patent claim 1.

Depending on the fault tolerance required of a communication device, different redundancy structures can bee **[sic]** provided for the peripheral line assemblies belonging thereto. Examples of this are the "1+1", "1:1", and "1:N" types of line assembly redundancy, as is described in "IEEE Journal on Selected Areas in Communications" (Vol. 15, N. 5, June 1997, pp. 795-806). In a "1+1" redundancy structure, two line assemblies are operated in parallel, in order to transmit message signal currents over them redundantly. But only one of these redundant message signal currents is considered for further processing.

In a "1+1" line assembly redundancy, only one of two line assemblies is used as the active line assembly, while a changeover onto the other line assembly, which serves as a back-up assembly, occurs only in case of a failure of the active line assembly.

Finally, in a "1:N" line assembly redundancy, in addition to a plurality N of line assemblies, a single backup line assembly is provided. When a failure occurs on one of the N line assemblies, the backup line assembly is then used instead.

In a "1:N" line assembly redundancy, a selector arrangement is typically connected between the line assemblies and external transmission lines, which arrangement can distribute individual transmission lines to the N lines assemblies and to the backup line assembly. But it must be noted that, when a selector arrangement such as this fails, or respectively, in a resulting replacement of this selector arrangement, all the transmission lines that are connected to it are interrupted, along with the connections running via these lines.

Beyond this, it is mentioned in the cited document that a transfer logic arrangement (LPS: Line Protection Switch) is connected on the output side of the communication device between the coupling field and the line assemblies, in order to be able to selectively realize the abovementioned redundancy structures. But more detailed information about the mode of functioning and the realization of this transfer logic arrangement is not given.

The US patent US 5,331,631 teaches a device with redundancy structure for trnasmitting message cells. The US patent 5,473,598 likewise teaches a redundancy structure for telecommunication systems. In both references, modifications are made to the routing information in case of a backup changeover.

It is the object of the invention to demonstrate how to construct the transfer logic arrangement that belongs to a communication device according to the preamble of patent claim 1 such that arbitrary redundancy structures can be realized with a low outlay in terms of control technology and circuitry.

This object is inventively achieved in a communication device according to the patent claim 1 by the wiring features cited in this claim.

The invention imparts the advantage that redundancy structures can be universally realized on the basis of the development of the transfer logic arrangement, without having to access redundancy-specific elements.

Advantageous developments of the invention derive from the subclaims.

The present invention is detailed below with the aid of drawings. These drawings illustrate only those elements which are necessary in order to gain an understanding the present invention.

Figure 1 sectional diagram of the schematic structure of a communication device according to the invention,

Figure 2 sectional diagram of the schematic structure of a coupling element that is detailed below, and

Figure 3 the schematic structure of a control device that is provided in the coupling element illustrated in Figure 2.

The communication device KE illustrated in Figure 1 is a matter of ATM communications equipment that functions in accordance with asynchronous transfer mode, enabling the transmission of message signals in the form of message cells in the course of virtual connections. Since the ATM principle and the general structure of message cells have long been known, these are not detailed here. It is merely noted here that the message cells appertaining to a virtual connection have an information part ("user part") and a cell header ("header") at their disposal, respectively. Among other things, a cell header like this contains what is known as a virtual channel number VCI, which references the respective virtual connection, and potentially what is known as a virtual path number VPI, a routing address that applies to the respective virtual connection, and what is known as housekeeping information, as well.

The communication device KE comprises a central coupling field ASN, which has at its disposal a central coupling arrangement ASN-C (ASN Core) with an appertaining coupling arrangement control ASN-CC, and at least one ATM multiplexer AMX that is connected to the coupling arrangement. This ATM multiplexer comprises a separate control, referenced AMX-C.

The communication device KE can be a matter of what is known as a cross connect for setting up virtual permanent connections, or a switching node for setting up virtual dial connections. In either case, the set-up of the connections is accomplished with the aid of said coupling arrangement control ASN-CC and of the control AMX-C. However, since this process of setting up virtual connections is not subject mater of the present invention, it is not discussed in greater detail here.

In the present exemplifying embodiment, a plurality of line assemblies are connected to the central coupling arrangement ASN via the ATM multiplexer AMX, via bidirectional electrical connections, for example. As illustrated im Figure 1, the ATM multiplexer can be designed for connecting 16 line assemblies, which are referenced LIC A0 to LIC A15. These line assemblies are provided for connecting at least one peripheral transmission line, respectively. The transmission lines, which may be designed for a bidirectional transmission of message signals, are referenced A1 to A15, according to their allocation to the line assemblies.

Incidentally, it should be noted that a plurality of ATM multiplexers AMX can also be connected to the central coupling arrangement ASN-C, depending on the required size of the communication device KE.

The ATM multiplexer AMX illustrated in Figure 1 comprises at least one separate coupling element SE for each direction of the transmission, which elements have a structure 16/16 in the present exemplifying embodiment; that is, they have 16 inputs and 16 outputs at their disposal. These coupling elements are controlled by the control AMX-C of the ATM multiplexer AMX. Among other things, the control consists in the specifying of a particular connection path via the respective coupling element in the course of the set-up of virtual connections. As previously mentioned, for such an established connection path, a specific routing address is contained in the cell header of the individual message cells, in order to make it possible to route the respective message cell via the relevant coupling element SE on the correct connection according to the specifications of this routing address.

As is described in detail below, control means are provided at least in the respective coupling element that is provided in the outgoing direction of transmission (that is, from the ATM multiplexer AMX to the line assemblies LIC A0 to LIC A15), so that, when one of the line assemblies fails, a backup path via the respective coupling

element is selected according to a specific redundancy structure, without it being necessary to change the routing address that is contained in the message cells that are to be transmitted via the backup path.

Figure 2 is a sectional illustration of the schematic structure of a coupling element SE for the outgoing direction of transmission. The backup switching principle just described is detailed with the aid of this Figure and Figure 3.

According to Figure 2, the illustrated coupling element SE, and every other coupling element, comprises a central cell memory ZP, in which the message cells that are to be routed via the line assemblies LIC A0 to LIC A15 are temporarily stored. Beyond this, the line assemblies LIC A0 to LIC A15 are each assigned an individual logical queue, these being referenced Q0 to Q15 according to their allocation to the individual line assemblies. These logical queues can be controlled individually according to the routing addresses contained in the message cells, and they serve for the temporary storage of address pointers, by means of which it is respectively indicated where in the cell memory ZP the message cells that are to be routed via the allocated line assembly are respectively stored. These address pointers are made available by the cell buffer ZP.

The logical queues Q0 to Q15 are processed – for instance, by a scanner (which is not illustrated) – cyclically in succession in a definite order, whereby one address pointer is extracted from each of the queues per cycle. Within the respective queue, the entered address pointers are read out in accordance with the FIFO principle. The address pointers that are loaded by the cell memory ZP are entered into the queues in question with the aid of a queue control QC. For this purpose, with each arrival of a message cell, this control is supplied at least with the part of the appertaining cell header in which the abovementioned routing address RA (Figure 2) is contained.

With the aid of this header, the queue into which the address pointer just loaded is to be entered is determined.

The above described controlling of the logical queues by the queue control QC is discussed below in detail with the aid of Figure 3.

The central part of the queue control QC is formed by a transfer logic arrangement LPS, by means of which one or more arbitrary queues of the queues Q0 to Q15, and thus one or more line assemblies LIC A0 to LIC A15, can be randomly allocated to each routing address RA. For this purpose, a register is kept in the transfer logic arrangement LPS for every routing address possibly contained in the message cells. In each of these registers, a separate bit position is reserved for each of the queues Q0 to Q15; that is, in the given example, there are 16 bit positions provided per register. The queue into which the address pointer that has been detected for a message cell is to be entered during the storing of this cell is indicated by a specified logic level, for instance "1", in one or more bit positions of a register. By contrast, a logic level "0" signifies that the allocated queue is blocked.

The individual registers can be individually controlled at least according to the abovementioned routing addresses RA, which are contained in the respective message cells. The controlling is accomplished with the aid of a control logic arrangement (which is referenced QA in Figure 3), to which the routing address that is contained in the appertaining cell header is delivered with each arrival of a message cell.

Furthermore, the register contents of the transfer logic arrangement LPS are preloaded jointly by the control unit AMX-C illustrated in Figure 1 (which process is not illustrated) when the communication device KE is initialized (Figure 1), or they are modified individually if necessary; that is, in a backup switching process as described above, for example.

It is illustrated again in Figure 3 that the individual queues Q0 to Q15 can be controlled individually by the transfer logic arrangement LPS in accordance with said register contents, in order to pick up the aforesaid address pointers for message cells that are stored in the cell buffer ZP (Figure 2).

The basic method of functioning of the devices illustrated in the Figures 1 to 3 having been hereby described, it is now explained how the abovementioned various redundancy structures can be realized with the aid of the cited register contents of the conversion arrangement LPS.

In a system without assembly redundancy, a system with a "1:1" assembly redundancy, or a system with a "1:N" assembly redundancy, the queue (Q0 to Q15) that is to be used for picking up an address pointer currently being made available, and thus ultimately the line assembly LIC A0 to LIC A15 via which the message cell that is allocated to the relevant address pointer is to be routed, is respectively indicated in the registers of the changeover logic arrangement LPS by a logical "1" at one of the bit positions only. The other bit positions of the individual registers are set to the logic level "0".

When it is necessary to perform a backup changeover of a faulty line assembly (LIC A0 to LIC A15), which assembly is identified by a specific routing address, it is merely necessary to provide the previously marked bit position in the register, which is allocated to this routing address, of the changeover arrangement LPS with a logic level "0", and to mark a bit position that pertains to the backup switching process with a logic level "1" instead.

When a "1+1" assembly redundancy is required, two – for instance, adjacent – bit positions in the registers of the changeover logic arrangement LPS are set to the logic level "1", respectively, in order to thereby mark the queues that are allocated to these

two bit positions as activated. This means that, with said storing of a message cell in the cell memory ZP (Figure 2), the address pointer that is allocated to the message cell being stored is simultaneously entered into both of the queues that are designated active.

In addition to the realization just described of different redundancy structures with the aid of specific register contents of the changeover logic arrangement LPS, a broadcasting can also be realized in that a logic level "1" are [sic] entered into all bit positions of the register, respectively. The result of this is that all of the message cells that are delivered by the coupling arrangement ASN are routed to all line assemblies (LIC A0 to LIC A15).

As mentioned above, besides a routing address, the cell headers of the message cells respectively contain what is known as housekeeping information, among other things. Among other things, this housekeeping information indicates the type of the respective message cell; that is, whether the respective message cell is a matter of a normal payload cell, or respectively, a connection-specific control cell, or it is a matter of a system-specific control cell. In this exemplifying embodiment, in order to be able to detect these cell types when a message cell occurs, a cell filter FIL is provided in the control logic arrangement LPS or is connected to the control logic arrangement LPS upstream. This cell filter is passed by the housekeeping information of received message cells, and the detected cell type is indicated. In accordance with the respectively detected cell type, only normal payload cells, or respectively, connection-specific control cells, are routed according to the specifications of the register contents of the control logic arrangement LPS. By contrast, system-specific control cells are forwarded without modification of the respective original connection path as characterized by a particular routing address. This can be accomplished in that, for example, the information (address pointer) that is required for the routing of such a control cell is entered directly into the required queue.